

FIG. 1B

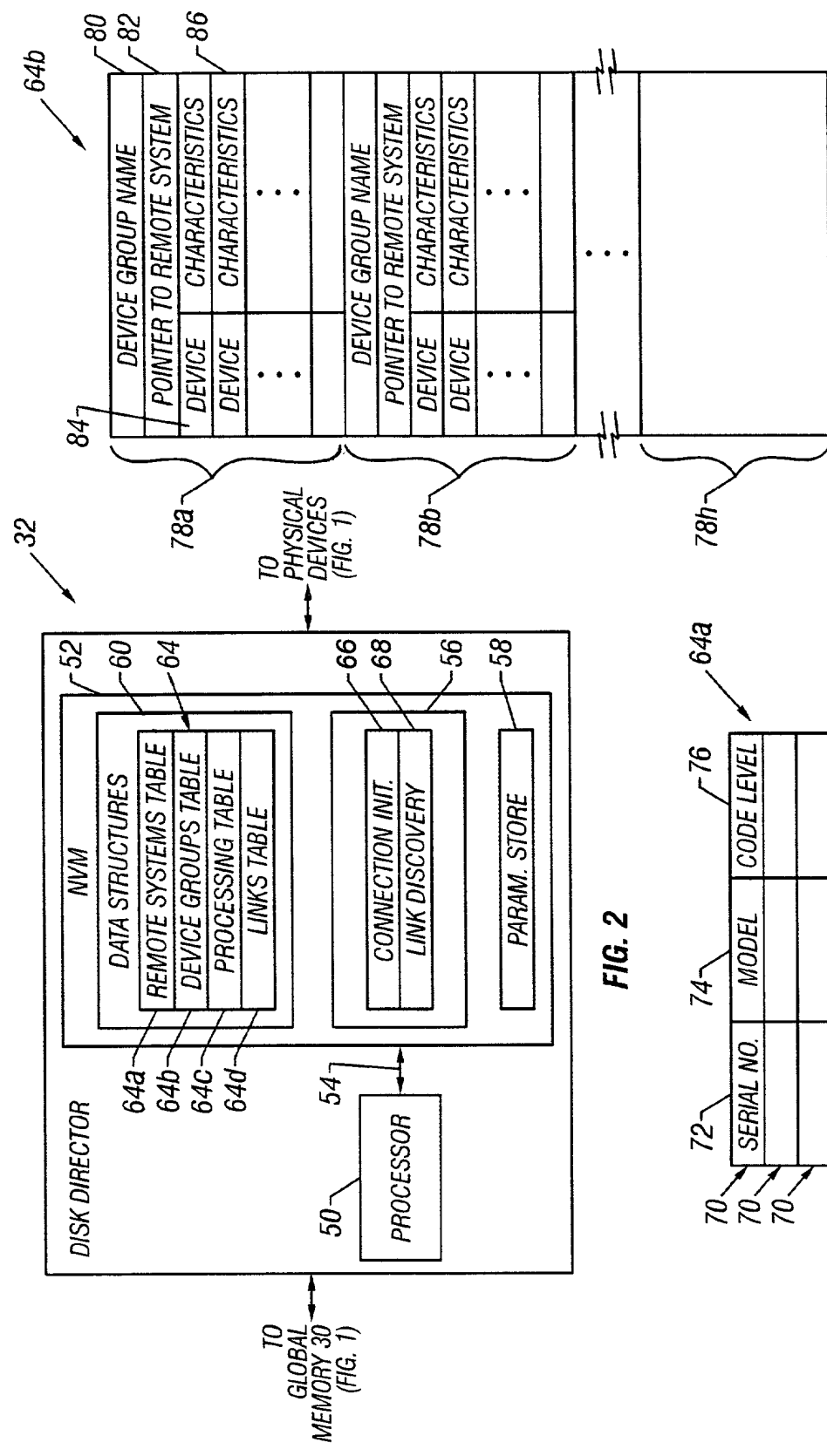


FIG. 2

FIG. 3B

FIG. 3A

70	72	74	76
SERIAL NO.	MODEL	CODE LEVEL	

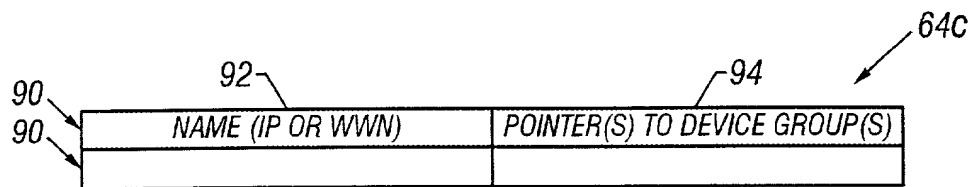


FIG. 3C

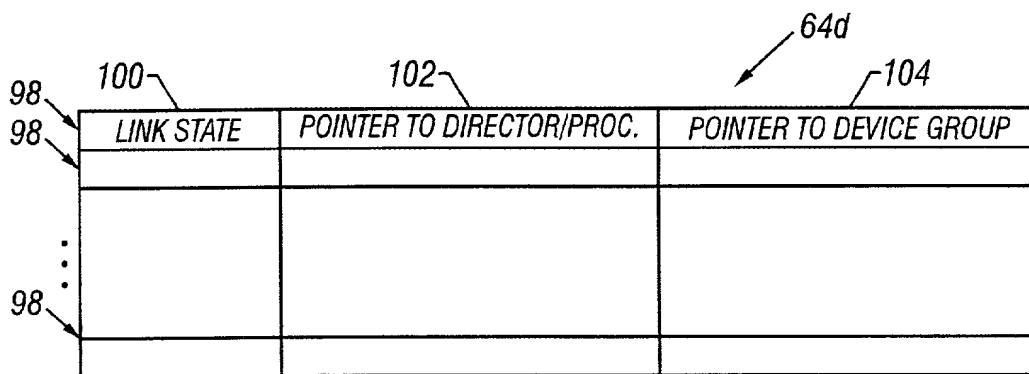


FIG. 3D

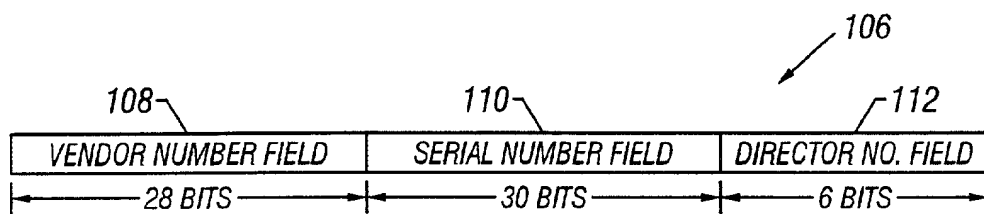


FIG. 4

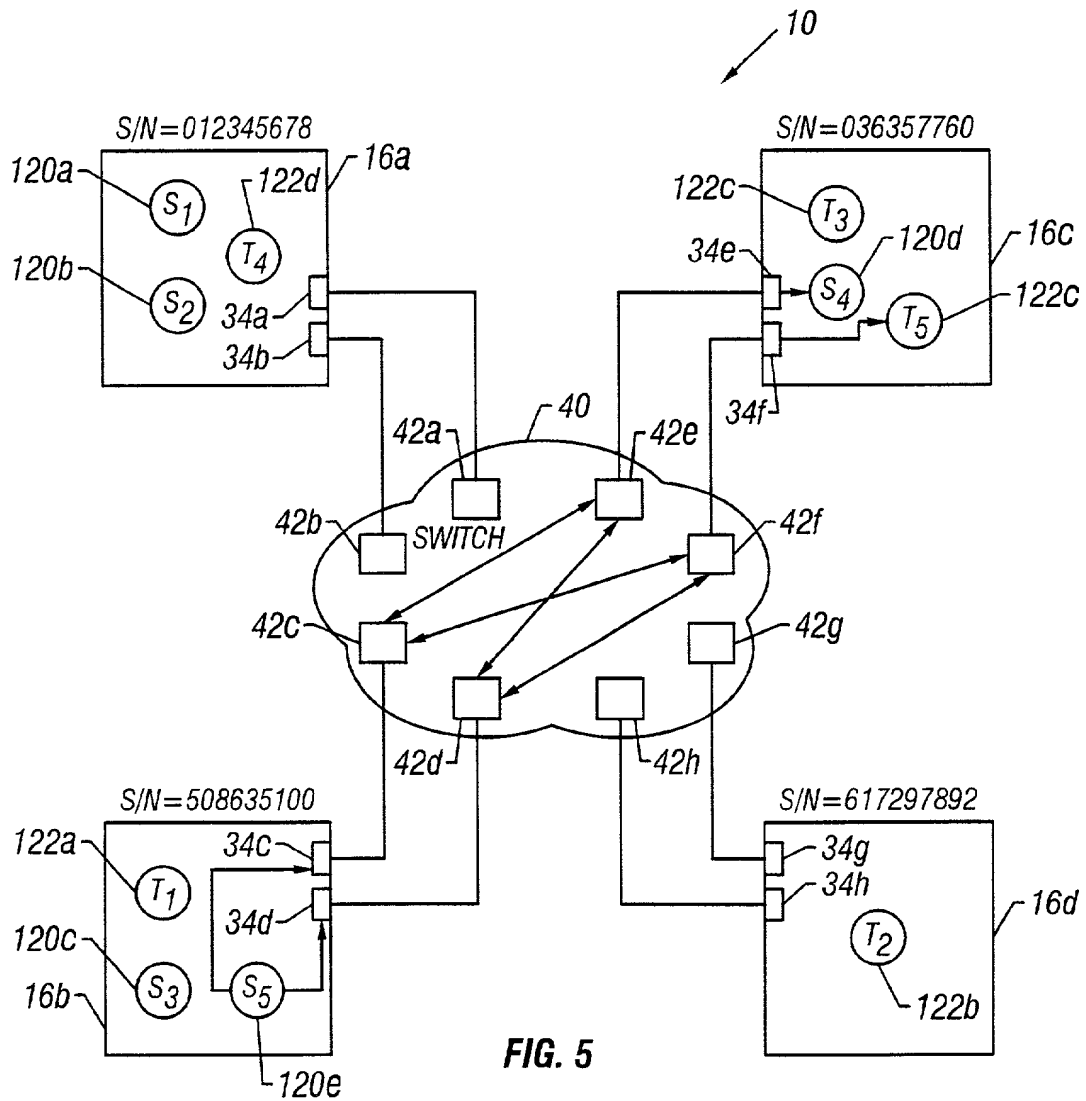


FIG. 5

FIG. 6 is a block diagram of a system architecture showing the flow of information from logical links through directors and device groups to remote box information.

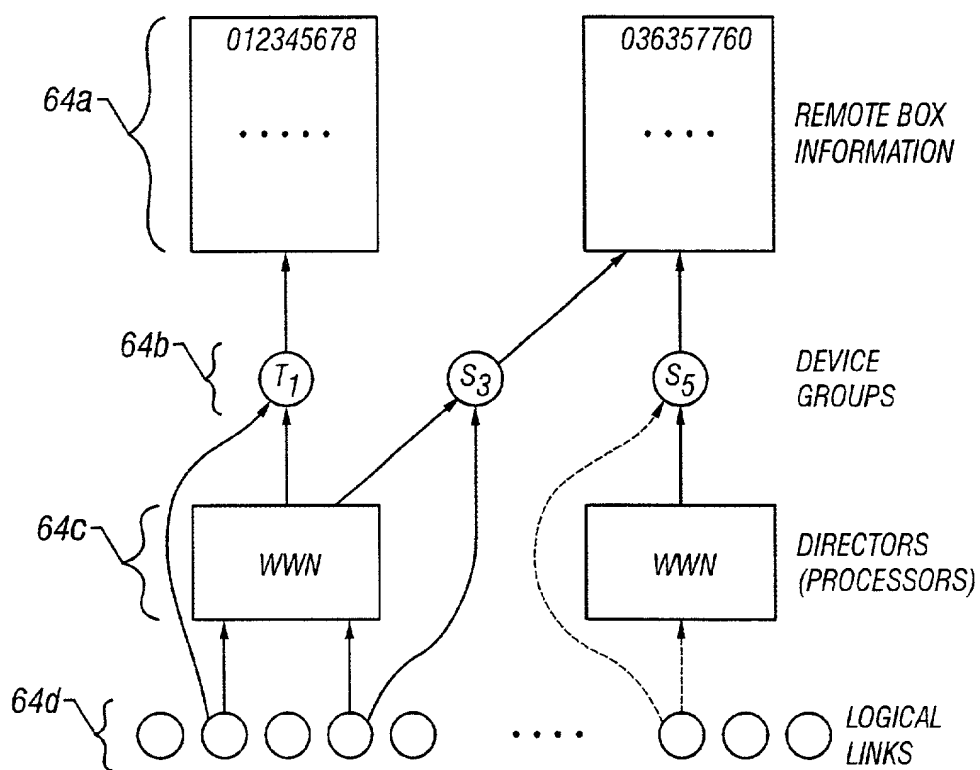


FIG. 6

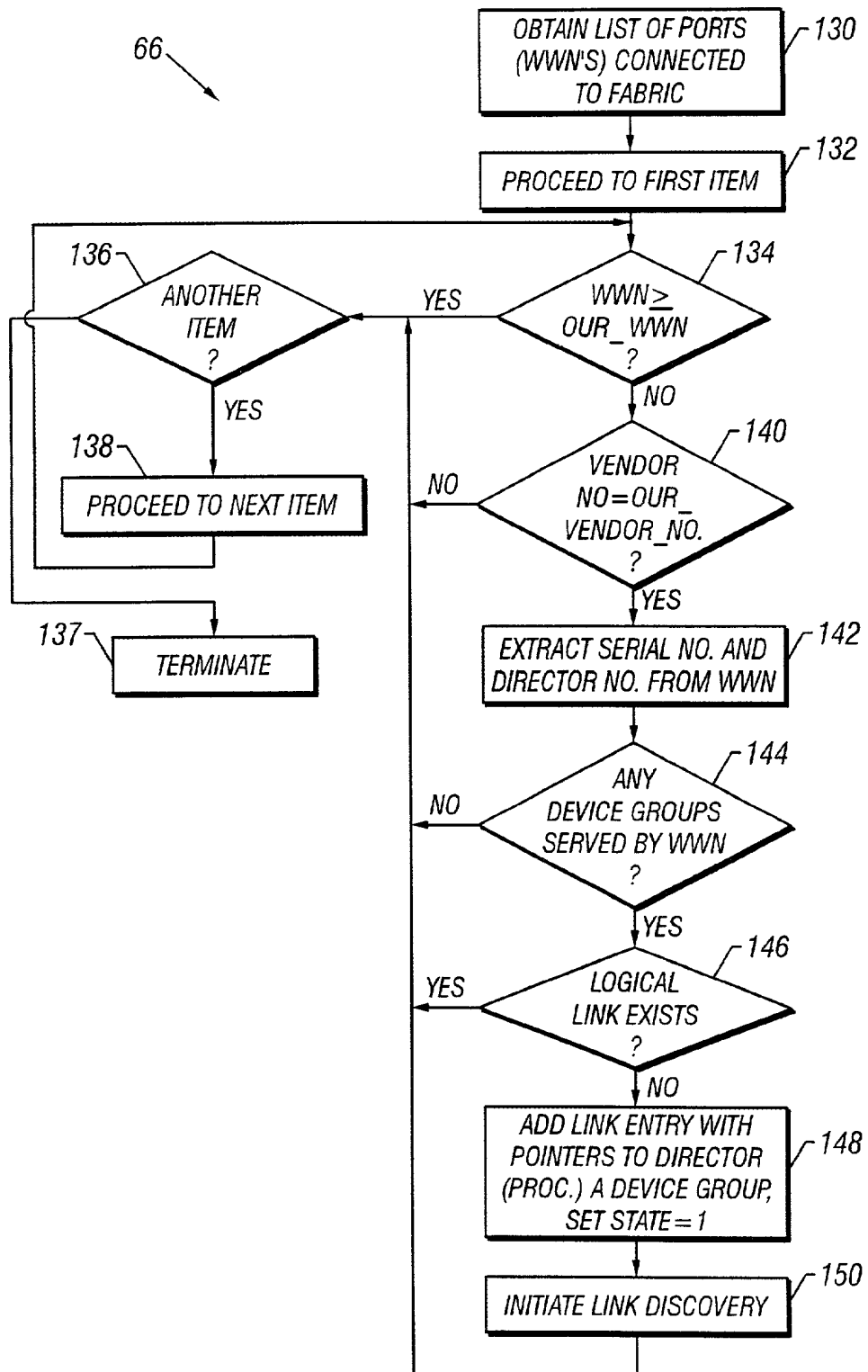


FIG. 7

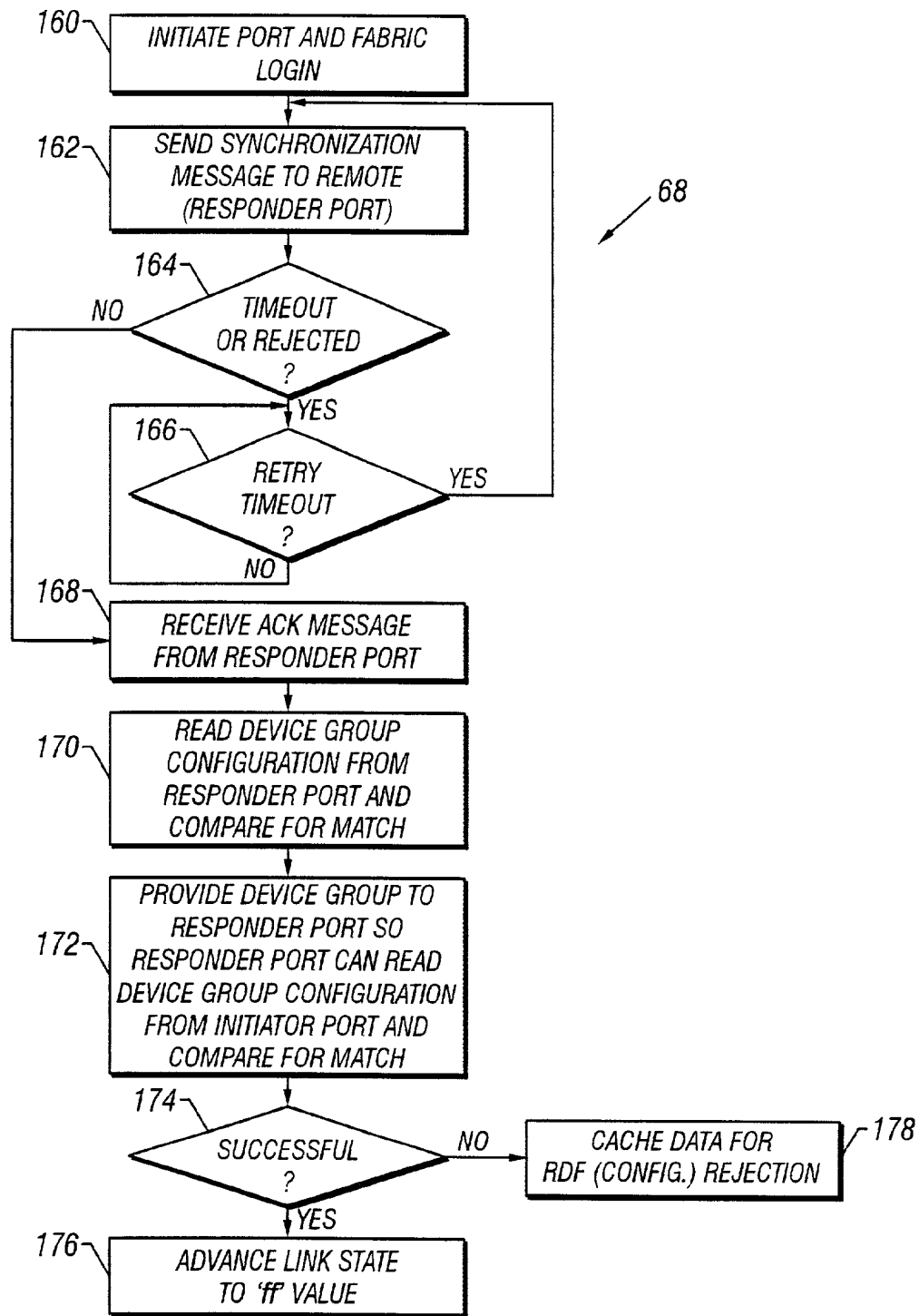


FIG. 8